What is claimed is:

1. A capacitive load driving circuit comprising:

an input terminal;

a front-edge delay circuit for delaying a front edge of an input signal input via said input terminal;

a back-edge delay circuit for delaying a back edge of said input signal;

an amplifying circuit for amplifying a drive control signal obtained through said front-edge delay circuit and said back-edge delay circuit; and

an output switch device which is driven by said amplifying circuit.

2. The capacitive load driving circuit as claimed in claim 1, wherein:

said front-edge delay circuit is a rising edge delay circuit for delaying a rising edge of said input signal; and

said back-edge delay circuit is a falling edge delay circuit for delaying a falling edge of said input signal.

3. The capacitive load driving circuit as claimed in claim 2, wherein said input signal is a positive polarity pulse signal.

4. The capacitive load driving circuit as claimed in claim 2, wherein said rising edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element and wherein, when said input signal rises, said capacitive element is charged through said resistive element and, when said input signal falls, said capacitive element is discharged through said switch element.

5. The capacitive load driving circuit as claimed in claim 4, wherein said switch element in said rising edge delay circuit is a diode.

6. The capacitive load driving circuit as claimed in claim 4, wherein the delay time of said rising edge

delay circuit is adjusted by varying the resistance value of said resistive element.

7. The capacitive load driving circuit as claimed in claim 4, wherein the delay time of said rising edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

8. The capacitive load driving circuit as claimed in claim 2, wherein said falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element and wherein, when said input signal falls, said capacitive element is charged through said resistive element and, when said input signal rises, said capacitive element is discharged through said switch element.

9. The capacitive load driving circuit as claimed in claim 8, wherein said switch element in said falling edge delay circuit is a diode.

10. The capacitive load driving circuit as claimed in claim 8, wherein the delay time of said falling edge delay circuit is adjusted by varying the resistance value of said resistive element.

11. The capacitive load driving circuit as claimed in claim 8, wherein the delay time of said falling edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

12. The capacitive load driving circuit as claimed in claim 1, wherein:

said front-edge delay circuit is a falling edge delay circuit for delaying a falling edge of said input signal; and

said back-edge delay circuit is a rising edge delay circuit for delaying a rising edge of said input signal.

13. The capacitive load driving circuit as claimed in claim 12, wherein said input signal is a negative polarity pulse signal.

14. The capacitive load driving circuit as claimed

in claim 12, wherein said rising edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element and, wherein when said input signal rises, said capacitive element is charged through said resistive element and, when said input signal falls, said capacitive element is discharged through said switch element.

15. The capacitive load driving circuit as claimed in claim 14, wherein said switch element in said rising edge delay circuit is a diode.

16. The capacitive load driving circuit as claimed in claim 14, wherein the delay time of said rising edge delay circuit is adjusted by varying the resistance value of said resistive element.

17. The capacitive load driving circuit as claimed in claim 14, wherein the delay time of said rising edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

18. The capacitive load driving circuit as claimed in claim 12, wherein said falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element and wherein, when said input signal falls, said capacitive element is charged through said resistive element, and when said input signal rises, said capacitive element is discharged through said switch element.

19. The capacitive load driving circuit as claimed in claim 18, wherein said switch element in said falling edge delay circuit is a diode.

20. The capacitive load driving circuit as claimed in claim 18, wherein the delay time of said falling edge delay circuit is adjusted by varying the resistance value of said resistive element.

21. The capacitive load driving circuit as claimed in claim 18, wherein the delay time of said falling edge delay circuit is adjusted by varying the capacitance value of said capacitive element.

22. The capacitive load driving circuit as claimed in claim 1, wherein:

said front-edge delay circuit is a first monostable multivibrator which is triggered by the front edge of said input signal; and

said back-edge delay circuit is a second monostable multivibrator which is triggered by the back edge of said input signal, and wherein said drive control signal is generated by combining an output signal of said first monostable multivibrator with an output of said second monostable multivibrator.

23. The capacitive load driving circuit as claimed in claim 1, wherein:

said front-edge delay circuit comprises a first capacitive element and a first series circuit having a first resistive element and a first switch element; and

said back-edge delay circuit comprises a second capacitive element and a second series circuit having a second resistive element and a second switch element and, wherein said first series circuit and said second series circuit are connected in parallel.

24. The capacitive load driving circuit as claimed in claim 23, wherein said first capacitive element and said second capacitive element are together constructed as one common capacitive element.

25. The capacitive load driving circuit as claimed in claim 23, wherein the delay time of the front edge of said input signal is adjusted by varying the resistance value of said first resistive element, and delay time of the back edge of said input signal is adjusted by varying the resistance value of said second resistive element.

26. The capacitive load driving circuit as claimed in claim 23, wherein said first switch element and said second switch element are diodes.

27. The capacitive load driving circuit as claimed in claim 1, wherein:

said front-edge delay circuit comprises a first resistive element and a first capacitive element; and

said back-edge delay circuit comprises a second capacitive element and a series circuit having a second resistive element and a switch element and, wherein said first resistive element and said series circuit are connected in parallel.

28. The capacitive load driving circuit as claimed in claim 27, wherein said first capacitive element and said second capacitive element are together constructed as one common capacitive element.

29. The capacitive load driving circuit as claimed in claim 27, wherein the delay time of the front edge of said input signal is adjusted by varying the resistance value of said first resistive element, and delay time of the back edge of said input signal is adjusted by varying the resistance value of said second resistive element.

30. The capacitive load driving circuit as claimed in claim 27, wherein the delay time of the front edge of said input signal is adjusted by varying the resistance value of said first resistive element, and thereafter, delay time of the back edge of said input signal is adjusted by varying the resistance value of said second resistive element.

31. The capacitive load driving circuit as claimed in claim 27, wherein said switch element is a diode.

32. The capacitive load driving circuit as claimed in claim 1, wherein:

said front-edge delay circuit comprises a first counter which starts to count a clock signal from the front edge of said input signal; and

said back-edge delay circuit comprises a second counter which starts to count said clock signal from the back edge of said input signal, and wherein the delay time of said front edge is adjusted by varying a count value of said first counter, and delay time of said

back edge is adjusted by varying a count value of said second counter.

33. The capacitive load driving circuit as claimed in claim 32, wherein said first counter and said second counter are formed on the same semiconductor integrated circuit.

34. The capacitive load driving circuit as claimed in claim 1, wherein:

said capacitive load driving circuit comprises a first and a second capacitive load driving circuit;

a first output switch device in said first capacitive load driving circuit is connected between a power line and a capacitive load; and

a second output switch device in said second capacitive load driving circuit is connected between said capacitive load and a reference voltage.

35. The capacitive load driving circuit as claimed in claim 34, wherein:

said capacitive load driving circuit further comprises a third and a fourth capacitive load driving circuit;

a third output switch device in said third capacitive load driving circuit is connected to said capacitive load via a first coil; and

a fourth output switch device in said fourth capacitive load driving circuit is connected to said capacitive load via a second coil.

36. The capacitive load driving circuit as claimed in claim 34, wherein said power supply line is a sustain power supply line of a plasma display apparatus.

37. A capacitive load driving circuit comprising:

an input terminal;

a front-edge delay circuit for delaying a front edge of an input signal input via said input terminal;

a pulse width adjusting circuit for

generating a drive control signal having a prescribed pulse width from a delayed signal obtained through said front-edge delay circuit;

an amplifying circuit for amplifying said drive control signal; and

an output switch device which is driven by said amplifying circuit.

38. The capacitive load driving circuit as claimed in claim 37, wherein:

said front-edge delay circuit comprises a resistive element and a capacitive element; and

said pulse width adjusting circuit is a monostable multivibrator.

39. The capacitive load driving circuit as claimed in claim 38, wherein the delay time of said input signal is adjusted by varying the resistance value of said resistive element in said front-edge delay circuit.

40. The capacitive load driving circuit as claimed in claim 38, wherein the delay time of said input signal is adjusted by varying the capacitance value of said capacitive element in said front-edge delay circuit.

41. The capacitive load driving circuit as claimed in claim 38, wherein the pulse width of said drive control signal is adjusted by varying a time constant and the like of said monostable multivibrator.

42. The capacitive load driving circuit as claimed in claim 37, wherein:

said front-edge delay circuit is a first counter for counting a clock signal; and

said pulse width adjusting circuit is a second counter for counting said clock signal, and wherein the delay time of said input signal is adjusted by varying a count value of said first counter, and the pulse width of said drive control signal is adjusted by varying a count value of said second counter.

43. The capacitive load driving circuit as claimed in claim 37, wherein:

said front-edge delay circuit is a rising edge delay circuit for delaying a rising edge of said input signal; and

said pulse width adjusting circuit is a monostable multivibrator.

44. The capacitive load driving circuit as claimed in claim 43, wherein said input signal is a positive polarity pulse signal.

45. The capacitive load driving circuit as claimed in claim 37, wherein:

said front-edge delay circuit is a falling edge delay circuit for delaying a falling edge of said input signal; and

said pulse width adjusting circuit is a monostable multivibrator.

46. The capacitive load driving circuit as claimed in claim 45, wherein said input signal is a negative polarity pulse signal.

47. The capacitive load driving circuit as claimed in claim 37, wherein:

said capacitive load driving circuit comprises a first and a second capacitive load driving circuit;

a first output switch device in said first capacitive load driving circuit is connected between a power line and a capacitive load; and

a second output switch device in said second capacitive load driving circuit is connected between said capacitive load and a reference voltage.

48. The capacitive load driving circuit as claimed in claim 47, wherein:

said capacitive load driving circuit further comprises a third and a fourth capacitive load driving circuit;

a third output switch device in said third capacitive load driving circuit is connected to said capacitive load via a first coil; and

a fourth output switch device in said fourth capacitive load driving circuit is connected to said capacitive load via a second coil.

49. The capacitive load driving circuit as claimed in claim 47, wherein said power supply line is a sustain power supply line of a plasma display apparatus.

50. A plasma display apparatus comprising:

a plurality of X electrodes;

a plurality of Y electrodes which are arranged substantially parallel to said plurality of X electrodes, and which produce a discharge between said plurality of Y electrodes and said plurality of X electrodes;

an X-electrode driving circuit which applies a discharge voltage to said plurality of X electrodes; and

a Y-electrode driving circuit which applies a discharge voltage to said plurality of Y electrodes, and wherein said X-electrode driving circuit or said Y-electrode driving circuit is constructed using a capacitive load driving circuit, wherein said capacitive load driving circuit comprises:

an input terminal;

a front-edge delay circuit for delaying a front edge of an input signal input via said input terminal;

a back-edge delay circuit for delaying a back edge of said input signal;

an amplifying circuit for amplifying a drive control signal obtained through said front-edge delay circuit and said back-edge delay circuit; and

an output switch device which is driven by said amplifying circuit.

51. A plasma display apparatus comprising:

a plurality of X electrodes;

a plurality of Y electrodes which are arranged substantially parallel to said plurality of X

electrodes, and which produce a discharge between said plurality of Y electrodes and said plurality of X electrodes;

an X-electrode driving circuit which applies a discharge voltage to said plurality of X electrodes; and

a Y-electrode driving circuit which applies a discharge voltage to said plurality of Y electrodes, and wherein said X-electrode driving circuit or said Y-electrode driving circuit is constructed using a capacitive load driving circuit, wherein said capacitive load driving circuit comprises:

an input terminal;

a front-edge delay circuit for delaying a front edge of an input signal input via said input terminal;

a pulse width adjusting circuit for generating a drive control signal having a prescribed pulse width from a delayed signal obtained through said front-edge delay circuit;

an amplifying circuit for amplifying said drive control signal; and

an output switch device which is driven by said amplifying circuit.